Notice of Allowability	Application No.	Applicant(s)	
	10/025,414	TSAI ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Appeal Brief filed on 17 November 2005*.

2. ☒ The allowed claim(s) is/are *1-6 and 11-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

The finality of the previous Office Action is hereby withdrawn in response to the merits of the Appeal Brief filed on 17 November 2005.

Examiner's Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jeanette Harms (35,537) on 23 February 2006.

The application has been amended as follows: Claims 7-10 have been cancelled.

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

Applicants' arguments and portions of the disclosure which are critical to the allowability of these claims are summarized below.

> (Specification, paragraph 0003) To resolve this problem, certain simulation tools have been provided that can verify the layout of a sub-wavelength integrated circuit compared to the printed wafer.

> (Specification, paragraph 0005) Thus, the simulation tool is inefficiently used to re-run simulations on the same design rather than running new designs.

(Specification, paragraph 0007) In accordance with one feature of the invention, a user can extract information from a database, which is generated by a one-time simulation of the user's layout.

(Appeal Brief, page 7) "In general, Lavenir [the applied prior art] teaches CAM software for printed circuit board (PCB) data (page 13), not for generating a report for an integrated circuit (IC) layout."

(Appeal Brief, page 7) "Because Lavenir teaches manipulating data at the board level, not at a sub-wavelength level, simulation is not necessary.

(Appeal Brief, pages 8-9) "In contrast, as taught by Appellants in the Specification (emphasis added) with respect to the recited database,

> [0029] If the deviation of a control point is greater than its tolerance (as determined by simulation module 102), then the deviation of this control point can be written to the database. Of importance, **the actual magnitude of the deviation as well its the direction** (wherein "+" indicates a deviation outside the feature as defined by the original layout and a "-" indicates a deviation inside the feature) **can be written to the database.** Note that **in current simulation tools the presence and location of the deviation can be accessed. However, the user is unable to access more in-depth information to facilitate more useful simulation results.**

Therefore, the simulation itself is not the object of Appellants' invention. Rather, the invention relates to a novel database that can capture information regarding that simulation to minimize the need to repeat the simulation process."

(Appeal Brief, page 10) "As taught by Appellants, in sub-wavelength designs, traditional design rule checking (DRC) tools cannot be relied upon as a final check for silicon manufacturability. Specification, paragraph [0002]. For this reason, simulation tools were developed. Specification, paragraph [0003]. Therefore, design rule checking (DRC) is not the same as simulation.

The "simulation" recited by the claims should be interpreted consistently with at least paragraphs 0003 through 0007 of the specification. The term "simulation" does not mean a "design rule check." The breadth of the term "simulation," as set forth by the specification and Appellants' arguments, is substantially "a simulation of an integrated circuit design at a sub-wavelength level" or equivalent.

The closest prior art of record teaches:

a design rule check without a "simulation" [*"[T]he features within the mask layout are checked using the selected rule, and any rule violations are marked in step 704."* (US Patent Application Publication US 2003/0061583 A1, paragraph 0058, etc.)];

a design rule check performed on a "simulation" [*"Optical rule checking (ORC) is performed at 740. In one embodiment, the ORC is performed on one or more simulated integrated device layers."* (US Patent 6,425,113, column 9, lines 56-59)];

requiring separate simulations for different tolerances [*"ORC component 460 analyzes the edge collection by simulating the performance expected on the wafer, and determining whether the wafer structures will violate a set of fabrication tolerances."* (US Patent 6,425,113., column 7, lines 22-30); *"The simulated etching image 626 represents an image transferred on a wafer after the wafer was exposed through the physical mask 604 wherein the wafer was ... etched in accordance with the etching process parameters 622."* (US Patent 6,757,645, column 16, lines 9-14)]; or

performing a simulation but subsequently attempting to automatically correct the detected errors [*"As IC designs become more complex, manual OPC (entering corrections by hand through trial and error) becomes more time consuming and less cost effective. Software modeling, or simulation, is a basis for one form of automated OPC referred to herein as model-based OPC. In model-based OPC, manufacturing distortions can be predicted and compensated for at the design stage by operating on edge fragments."* (US Patent 6,467,076, column 2, lines 22-30)].

None of these references taken either alone or in combination with the prior art of record disclose a method of generating simulation reports regarding an integrated circuit layout, the method specifically including:

(Claim 1, 17) "performing a single simulation of the plurality of control points; storing information from the single simulation in a database, wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and extracting a subset of information from the database to generate the reports using a first set of checking parameters, wherein extracting is repeatable with a second set checking parameters without repeating the steps of providing, performing, and storing" or

(Claim 11) performing a single simulation of the integrated circuit layout using the control points; storing simulation information in a database, wherein the simulation information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and extracting user-identified information from the database to generate the simulation reports"

in combination with the remaining elements and features of the claimed invention. It is for these reasons that the Applicants' invention defines over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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